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REMARKS

The applicant respectfully traverses the above rejections with the following arguments.

Claims 1-7 and 15-27 stand rejected under 35 U.S.C. § 102(b) as unpatentable over Stoica et al., "Evolutionary Design of Electronic Devices and Circuits, Evolutionary Computation" IEEE CEC 99, July 1999.

First, from a general perspective, applicant notes that the subject matter contained in Stoica et al. (of which applicant is a co-author) is the basis of the subject matter of the parent application to which the present application is a continuation-in-part. The subject matter of the parent application is described in pages 10-23 of the present application, which describes the subject matter found in Stoica et al. The newly added subject matter of the present application (that not described in either Stoica et al. or the parent application) is described on pages 23-31 of the present application.

Pages 23-25 of the present application, describe that the new subject matter of the present application was developed to overcome problems with using conventional modeling techniques. These techniques would include those described in the parent application and Stoica et al. For proof of this assertion, applicant directs the examiner to the descriptive example, and associated problems, on page 23, line 23 through page 25, line 9.

As the examiner notes in the present Action, since the claims of the present application are based on new subject matter, outside of the original matter of the parent application, the Stoica et al. reference may be used as a reference against the present continuation-in-part application. In order to make a proper rejection under 35 U.S.C. 102(b), every limitation of the claims must be set forth in the reference. Since the examiner specifically states that the present claims contain matter not found in the parent application, the only way for the Stoica et al.

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reference to properly be used to make a 102(b) rejection would be if the reference contained the matter that was added to the present application, not originally found in the parent application.

However, based upon the above description (and the specification of the present application) this assertion is illogical. As described above, the new matter added to the present application is a result of inventive steps developed to address the problems associated with the Stoica et al. reference. If the Stoica et al. reference contains said matter, there would be no "problem" to overcome in the modeling techniques in Stoica et al. However, the present specification describes, in detail, these problems as well as how the newly developed inventive steps overcomes the problems.

More particularly, the examiner indicates that all of the elements within the claims are disclosed in the reference, including modeling many or all candidate solutions at various levels of "resolution" and combining the fitness functions to arrive at a high quality solution in a reasonable amount of time. Specifically, the examiner states that "SPICE simulation software has many levels of models for transistors for different levels of resolution or accuracy..."; "Therefore, depending on interest in level of accuracy, a model is assigned to one or more or all transistors in a circuit."; and "As a result, the examiner interprets that assigning different levels of model resolution to different circuits inherits from SPICE."

Applicant asserts that the examiner has misinterpreted the limitations found within the claims, and, therefore, certain limitations found within the claims are not present in the Stoica et al. reference. While SPICE simulation software allows a user to select a specific resolution to run a simulation (as is noted in the present specification on pages 23-25), the limitation within the claims at issue is not merely to "assign a resolution level" (which is actually done in every simulation as is described in numerous references and the specification of the present

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application— and relates to the entire problem that the present invention has been developed to resolve), but to run simulations for a circuit at a plurality of resolution levels and use the data obtained from these simulations to obtain a preferred solution. Again, this is extremely different than running a simulation at a selected resolution and continually throwing out "bad" data to obtain a solution (which is the standard simulation method).

Thus, while applicant agrees with the examiner that SPICE software allows a user to select different resolution levels and that assigning a resolution level is inherent in the software, these features of the software do not provide the limitations found within the claims (which are to run simulations at a plurality of resolutions and use that data to obtain the preferred solution). Because these limitations are not found in the Stoica et al. reference, any anticipation rejection is improper.

Claims 8-14 also stand rejected 35 U.S.C. § 103(a) as unpatentable over Stoica et al. in view of Koza et al., "Automated Synthesis of Computational Circuits Using Genetic Programming", 13-16 April 1997, IEEE Conference. Specifically, the examiner indicates that the Stoica et al. reference discloses all of the limitations except combining the plurality of fitness functions into a single fitness function, which is disclosed by Koza et al.

The examiner indicates that p. 449, col. 1, lines 51-61 and col. 2, line 1 disclose the above. The Koza et al. reference (which was supplied by the applicant) is not paginated, and, therefore, applicant does not understand these reference points. Regardless, what Koza et al. discloses is merely applying functions to a circuit-constructing program tree that inserts components into the tree. Fitness functions are applied to each potential change in components and the preferred components are selected. This is merely the standard methodology used in

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genetic programming. The reference does not disclose anything more than that of the Stoica et al. reference as it applies to fitness functions.

The limitations in the claims at issue combine fitness functions from simulations at different resolutions. Neither of the references disclose combining fitness functions obtained by running simulations at a plurality of resolutions. The mere fact that a reference may disclose a method of combining functions to obtain a single solution (which has been done mathematically for hundreds of years) is not particularly relevant to the present invention. The unique limitations of the present invention relate to the selection of a plurality of simulation runs at different resolution levels (both high and low resolutions) and combining fitness functions from these runs in order to obtain a preferred solution (which, inherently, takes into account aspects of both the higher and lower resolution solutions in order to get a "good" solution in a reasonable amount of time). Therefore, since neither of the references discloses these limitations or concepts, an obviousness rejection based upon these references is improper.

Accordingly, applicant believes that claims 1-27 are in condition for allowance and respectfully requests the examiner to withdraw all objections and rejections and allow said claims. Should the examiner need more information regarding this matter or have further suggestions regarding this application, feel free to call the undersigned at 818-354-7770.

                                    Respectfully submitted,

                                    Mark Homer

                                    Mark Homer, Reg. No. 41,848
                                    Attorney for Applicant

NASA Management Office
Jet Propulsion Laboratory
Mail Stop 180-200
4800 Oak Grove Drive
Pasadena, CA 91109-8099